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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,872	KANAMORI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8-20,22,24,25 and 27-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *38 and 39* is/are allowed.

6)☒ Claim(s) *6,25 and 40* is/are rejected.

7)☒ Claim(s) *1,3,5,8-20,22,24,25 and 27-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 10/28/05. Note that, based on applicant's persuasive argument, the rejections under 35 U.S.C. 112, 1st paragraph, in the last office action have been withdrawn.

Claim Objections

2. Claims 1, 3, 5, 6, 8-16-19, 20, 22, 24, 25 and 27-37 are objected to because of the following informalities:

Claim 1, line 11, "first level said" should be changed to --first level, said--.

Claims 3, 5, 6, and 8-16 are objected to because they include the informality of claim 1.

Claim 17, line 4, "generated" should be deleted.

Claims 18, 19, 22, 24, 25 and 27-35 are objected to because they include the informality of claim 17.

Claim 19, line 3, "the amplifier" should be changed to --the differential amplifier--.

Claim 20, line 11, "a clock and supplying the generated clock to" is suggested to be changed to --a clock signal and supplying the clock signal to-- for clarity.

Also, in claim 20, line 20-21, the phrase "are connected, wherein said third transistor also supplies a drive current at the time of signal determination" is suggested to be changed to --are connected in response to a first level of the clock signal, wherein said third transistor supplies a drive current in response to a second level of the clock signal—to avoid a confusion in the meaning of "at the time of signal determination" in the above phrase, so that the claim is clear.

Claim 33, line 3-4, "a differential output signal" should be changed to --the output signal of said differential amplifier circuit-- to avoid unclear antecedent basis (see line 3 of claim 17).

Claim 36, line 14, "the Inter-Symbol" should be changed to --an Inter-Symbol-- to avoid lacking antecedent basis.

Claim 37 is objected to because it includes the informality of claim 36.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 6, the recitation "wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor" recited in claim 6 appears to be misdescriptive since, according to the disclosure, the above recitation applies the embodiments of Figures 8, 9 and 13-17 (i.e., third transistor 3 having a smaller gate width than fourth transistor 30 in Figures 8, 9 and 13-17). However, the third transistor 3 in those Figures does not provides the function of supplying a minute current at a first level of the clock/control signal and a first drive current at a second level of the clock/control signal. Note that, in the newly added Figures 26-32 which replaces the minute current transistor 3 with transistor 30' wherein transistors 30' provides both the minute current at a first level of the clock/control signal and the first drive current at a second level of the clock/control signal, the original disclosure does not disclose that transistor 30'

having a smaller gate width than transistor 30. Clarification and/or appropriate correction is requested.

With respect to claim 25, the recitation "wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor" is indefinite for the same reason as discussed in claim 6.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Itou (USP 5,903,513).

With respect to claim 1, each of the Figures 1-6 of the applicant's admitted prior art shows a differential sense amplifier circuit which includes: a latch unit (111, 112, 121, 122); and a differential input portion (101, 102) comprises a first transistor (101) and a second transistor (102); and a current device (130 including a third transistor (130). Each of the Figures 1-6 of the applicant's admitted prior art does not disclose that the third transistor (130) for keeping a minute current to flow through the differential input portion in response to a first level of a control signal, and also for supplying a drive current in response to a second level of the control signal. However, Figure 7 of the Itou reference disclose a differential amplifier circuit (61) which includes current device (74) including a third transistor (71) for keeping a minute current (i.e., when clock CLKH is low, transmission gate 72 is on so the gate of transistor 71 receives the

lower reference voltage VaL, so there is a smaller current (minute current)) to flow through the differential input portion of the differential amplifier, and also for supplying a drive current at the time of signal determination for the differential amplifier (i.e., when clock CLKH is Hi, transmission gate 73 is on so the gate of transistor 71 receives the higher reference voltage VaH, so transistor 71 supplies a larger current (drive current) for the differential amplifier) for the purpose of controlling the gain of the differential amplifier (see lines 6-53 of Col. 12 of Itou) and reduce the power consumption of the amplifier (see line 15-16 of Col 13 of Itou). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the differential amplifier in each of the Figures 1-6 of the applicant's admitted prior art to replace the current device (130) by the current device (74, Figure 7 of Itou) as taught by the Itou reference for the purpose of controlling the gain of the differential amplifier and reduce the power consumption of the differential amplifier. Thus, each of these combination/modification meets all the limitations of claim 40 because the third transistor (transistor 71 in the above combination/modification) for keeping a minute current to flow (when CLKH is low, gate of transistor 71 receives a lower reference VaL to provides the minute current as discussed above) and also for supplying a drive current (when CLKH is Hi, gate of transistor 71 receives a higher reference VaH to provide the drive current as discussed above, and the drive current is larger than the minute current as discussed above).

7. Claim 40 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Branson et al. (USP 5,508,664) in view of Itou (USP 5,903,513).

With respect to claim 40, Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10), which includes: a latch unit (12, 14, 16, 18) and a differential input

portion (22, 20) comprising a first transistor (22) and a second transistor (20), and a current device (parallel connected transistors 26 and 24) comprising a transistor (26) for supplying the minute current (small current that transistor 26 sinks, see lines 5-6, Col. 3) and a transistor (24) for supplying a drive current at the time of signal determination (i.e., when LE is Hi). The Branson et al. reference does not discloses

a third transistor for keeping a minute current to flow through the differential input portion in response to a first level of a control signal, and also for supplying a drive current in response to a second level of the control signal. However, Figure 7 of the Itou reference disclose a differential amplifier circuit (61) which includes current device (74, Figure 7) including only one transistor (71) for keeping a minute current (i.e., when clock CLKH is low, transmission gate 72 is on so the gate of transistor 71 receives the lower reference voltage VaL, so there is a smaller current (minute current)) to flow through the differential input portion of the differential amplifier, and also for supplying a drive current at the time of signal determination for the differential amplifier (i.e., when clock CLKH is Hi, transmission gate 73 is on so the gate of transistor 71 receives the higher reference voltage VaH, so transistor 71 supplies a larger current (drive current) for the differential amplifier) instead of using two parallel connected transistors (current device 58, Figure 4-5, see Col. 10, lines 49-54, Itou) and provides advantage of reducing the power consumption of the amplifier (see line 15-16 of Col 13 of Itou). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the differential amplifier 1 of Branson et al. to replace the current device (parallel connected transistors 26 and 24, Figure 1 of Branson et al.) by the current device (74, Figure 7 of Itou) as taught by the Itou reference for the purpose of reducing the power consumption of the

differential amplifier. Thus, each of these combination/modification meets all the limitations of claim 40 because the third transistor (transistor 71 in the above combination/modification) for keeping a minute current to flow (when CLKH is low, gate of transistor 71 receives a lower reference VaL to provides the minute current as discussed above) and also for supplying a drive current (when CLKH is Hi, gate of transistor 71 receives a higher reference VaH to provide the drive current as discussed above, and the drive current is larger than the minute current as discussed above).

Allowable Subject Matter

8. Claims 38 and 39 are presently allowed. Claims 1, 3, 5, 8-20, 22, 24 and 27-37 would be allowed if amended to overcome the informalities set forth above.

Response to Arguments

9. Applicant's arguments filed on 10/28/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Because the scope of claims 6 and 25 cannot be determined due to the indefiniteness set forth above, the indication for allowability of these claims are not appropriate at this time.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 4, 2006

LONG NGUYEN
PRIMARY EXAMINER